REMARKS

Reconsideration is requested.

An election is being required between Species 1 and Species 2. Species 1 is hereby elected for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable. Claims 50-60 have been canceled.

Claims 11-15 stand rejected under 35 U.S.C. 101, "same invention" type double patenting as being unpatentable over claims 18-36 of prior allowed Application No. 09/388,856.

A "same invention" double patenting rejection requires identical subject matter. According to the MPEP, the test is whether there is an embodiment of the invention that falls within the scope of one claim, but not the other. If there is such an embodiment, then identical subject matter is not defined by both claims and statutory double patenting would not exist.

Claim 11 of the present application recites "devices" while claims 18-36 of application Serial No. 09/388,856 variously recite n-type transistor devices. Therefore, claim 11 is of different scope than claims 18-36 of the prior application.

Claims 12-15 of the present application variously recite "field effect transistors" while none of claims 18-36 of the prior application specifically recite "field effect" transistors.

Therefore, the "same invention" type double patenting rejection is improper and should be withdrawn.

Claims 5-10 stand rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,534,449 to Dennison et al. The Examiner has referred to Col. 2, lines 50-65 and Fig. 2 (26), (18) and (22). This rejection is respectfully traversed.

Claim 5 recites a semiconductor processing method comprising a masking step providing a common mask; and an implant step carried out through the common mask, comprising conducting a halo implant of devices formed over a substrate comprising memory circuitry and peripheral circuitry sufficient to impart to at least three of the devices three different respective threshold voltages.

The Dennison et al. reference fails to teach or suggest conducting a halo implant of devices formed over a substrate comprising memory circuitry and peripheral circuitry sufficient to impart to at least three of the devices three different respective threshold voltages, in combination with the other features of claim 5.

Instead, the method disclosed in the Dennison et al. '449 reference would result in devices having two different threshold voltages. More particularly, Fig. 2 of the Dennison et al. reference shows areas 26 and 22 that are completely masked by masking layer (38) and area 18 that is not masked. The areas 26 and 22 are both similarly masked and would not result in devices having different threshold voltages. Therefore, claim 5 is allowable. As claims 6-15 depend on claim 5, they too are allowable.

In view of the foregoing, allowance of claims 5-15 is respectfully requested.

A telephonic interview is requested in the event that the next Office Action is one other than a Notice of Allowance. The undersigned is available for telephone consultation at any time.

Respectfully submitted,

Dated: January 20, 2003 By: _____

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Reg. No. 33,560

Application Serial No. 09/848,846
Filing Date ..... May 3, 2001
Inventor ..... Luan C. Tran
Assignee ..... Micron Technology, Inc.
Group Art Unit 2813
Examiner ..... Laura M. Schillinger
Attorney's Docket No. MI22-1689
Title: Semiconductor Processing Methods of Forming Integrated Circuitry

VERSION WITH MARKINGS TO SHOW CHANGES MADE ACCOMPANYING RESPONSE TO OCTOBER 24, 2001 OFFICE ACTION

In the Claims

The claims have been amended as follows. Underlines indicate insertions and ~~strikeouts~~ indicate deletions.

Claims 50-60 have been canceled.

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